FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

Applicant:	K. Azadet, E.F. Haratsch
Case:	10-2
Serial No.:	09/471,920
Filing Date:	December 23, 1999
Group:	~~2739~~ 2631

#3

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	1.	Fettweis et al., "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture," IEEE Communications Magazine, May 1991.
	2.	Chevillat et al., "Decoding of Trellis-Encoded Signals in the Presence of Intersymbol Interference and Noise," IEEE Transactions on Communications, Vol. 37, No. 7, July 1989.
	3.	Erich F. Haratsch, "High-Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA.
	4.	K. Azadet, "Gigabit Ethernet over Unshielded Twisted Pair Cables," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA.
	5.	Black et al., "A 140-Mb/s, 32-State, Radix-4 Viterbi Decoder," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992.
	6.	Cypher et al. "Generalized Trace-Back Techniques for Survivor Memory Management in the Viterbi Algorithm*," Journal of VLSI Signal Processing, 5, 85-94(1993).

Phuong Phan — 2/11/03

Examiner — Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

#5

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
	5,870,433	2/9/99	Huber et al.		
	6,035,006	3/7/00	Matui		
	6,201,831	3/13/01	Agazzi et al.		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	NO

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	1.	Keshab K. Parhi, "Pipelining in Algorithms with Quantizer Loops," IEEE Transactions on Circuits and Systems, Vol. 38. No. 7, 745-754 (July 1991)
	2.	Bednarz et al., "Design, Performance, and Extensions of the RAM-DFE Architecture," IEEE Transactions on Magnetics, Vol. 31, No. 2, 1196-1201 (March 1995)

Phuong Phu — 02/11/03

Examiner — Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.